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EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/638,268	BRYAN ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 August 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' Response mailed on March 23, 2004. Claims 4 and 13 were amended. Claims 17-21 were added. Claims 1-21 of the application are pending. This office action is made non-final.

Response to Arguments

2. Applicants' amendments filed on March 23, 2004 have been fully considered. Claim rejections under 35 USC 112 Second Paragraph are withdrawn in response to Applicant's amendments to the claims. New claim rejections under 35 USC 112 First Paragraph and Second Paragraph are included in this Office Action covering the new claims. Claim rejections under 35 USC 103 (a) using additional prior art are included in this office action. Examiner's response to Applicant's arguments is presented in Paragraph 17 below.

Drawings

3. The drawings are objected to; see a copy of Form PTO-948 sent with previous Office action, Paper No. 4.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. §112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 20 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 20 states in part, "the command statement identifies a significance level with each parameter combination". There is no support for a significance level for each parameter combination in the specification. The specification describes the significance level and how it is used on pages 11 and 12 of the specification. The usage indicates that a significance level is associated with each parameter as shown in the example on page 12.

6. Claim 21 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 21 states in part, "the generator generates ***a transaction from each parameter*** of the command statement beginning with the lowest level of significance". There is no support for generating a transaction (bus transaction or a test case) from each parameter of the command statement in the specification. Therefore one of ordinary skill in the art will not know how to generate ***a transaction from each parameter***. A transaction involves a combination of parameters and specific values for the parameters. The claim appears to be incorrect. It is not clear as to how "beginning with the lowest level of significance" is used in generating the transaction if a transaction is generated for each parameter. It is also not clear as to what the lowest level of significance refers to.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 20 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 20 recites, "the command statement identifies a significance level with each parameter combination ". The significance level for each parameter combination is vague and indefinite since it is not described in the specification.

Claim 21 recites, "the generator generates ***a transaction from each parameter*** of the command statement beginning with the lowest level of significance". A

transaction from each parameter is vague and indefinite since it is not described in the specification. It is also not clear as to what the lowest level of significance refers to.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

10. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. Claims 1, 3-5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hellestrand et al. (HE)** (U.S. Patent 6,263, 302) in view of **Apostol, Jr. et al. (AP)** (U.S. Patent 6,247,084) and **Sheafor et al. (SH)** (U.S. Patent 6,321,285), and further in view of **Huggins (HU)** (U.S. Patent 5,956,478).

11.1 **HE** teaches hardware and software co-simulation including simulating the cache of a target processor. Specifically as per Claim 1, **HE** teaches providing a design-under-test (DUT) configuration file comprising a specification of cache model and parameters of the cache model and its operations corresponding to the DUT (CL14, L57 to CL15, L5; CL15, L50-58; CL16, L48 to CL17, L38); and a co-simulation design system that provides for accurately simulating some of the bus transactions using a bus hardware model where the user may select the bus transactions to simulate (Fig 1, Item 124; Fig 16, Item 1603 and 1605; CL10, L23-32). **HE** does not expressly teach providing a design-under-test (DUT) configuration file comprising a specification of bus transaction types and parameters corresponding to the DUT. **AP** teaches providing a specification of bus transaction types (Figs 8, 9 and 10; CL10, L55-60), as the bus supports different transaction types (CL10, L55). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of **HE** comprising a design-under-test (DUT) configuration file comprising a specification of the model and parameters of the model and its operations corresponding to the DUT and a co-simulation design system that provides for accurately simulating some of the bus transactions using a bus hardware model with the method of **AP** that included providing a specification of bus transaction types, as the bus would support different transaction types and the combination would allow the user to select the bus transactions to simulate using the specifications in the configuration file.

SH teaches providing a specification of bus transaction parameters (CL10, L44-67; CL11, L7-14), as the bus transaction parameters allow to appropriately configure the transaction to improve the efficiency of bus utilization (CL10, L48-50; CL11, L8-11). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the

method of **HE** comprising a design-under-test (DUT) configuration file comprising a specification of the model and parameters of the model and its operations corresponding to the DUT and a co-simulation design system that provides for accurately simulating some of the bus transactions using a bus hardware model with the method of **SH** that included providing a specification of bus transaction parameters, as the bus transaction parameters would allow to appropriately configure the transaction to improve the efficiency of bus utilization.

HE teaches providing a design-under-test (DUT) configuration file comprising a specification of cache model and parameters of the cache model and its operations corresponding to the DUT (CL14, L57 to CL15, L5; CL15, L50-58; CL16, L48 to CL17, L38); and a co-simulation design system that provides for accurately simulating some of the bus transactions using a bus hardware model where the user may select the bus transactions to simulate (Fig 1, Item 124; Fig 16, Item 1603 and 1605; CL10, L23-32). **AP** teaches providing a specification of bus transaction types (Figs 8, 9 and 10; CL10, L55-60). **SH** teaches providing a specification of bus transaction parameters (CL10, L44-67; CL11, L7-14). **HE, AP** and **SH** do not expressly teach processing the configuration file to generate a test case comprising bus transactions for verification of the DUT. **HU** teaches processing the configuration file to generate a test case for verification of the DUT (CL1, L64 to CL2, L5; CL2, L36-45), as that allows generating the tests in reduced time and the tests would exercise the device in a manner that was close to actual operation (CL2, L39-42), allowing the user to verify that the device meets all its functional requirements (CL2, L3-5). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the methods of **HE, AP** and **SH** comprising a

configuration file comprising bus transactions for verification of the DUT with the method of **HU** that included processing the configuration file to generate a test case for verification of the DUT, as that would allow generating the bus transactions tests in reduced time and the tests would exercise the device in a manner that was close to actual operation allowing the user to verify that the bus transactions meet all functional requirements.

Per Claim 3: **HE** teaches that the processing step comprises converting the specification into a plurality of combinations of the parameters (CL14, L57 to CL15, L5; CL15, L50-58; CL16, L48 to CL17, L38).

Per Claim 4: **HE** teaches applying the bus transactions to the DUT for verification (Fig 1, Item 124; Fig 16, Item 1603 and 1605; CL10, L23-32).

Per Claim 5: **HE** teaches describing a DUT in a configuration file using a condensed syntax (CL14, L57 to CL15, L5; CL15, L50-58; CL16, L48 to CL17, L38).

HE teaches verification of the DUT by converting the condensed syntax into an enumeration of possible parameter combinations for cache operations of the DUT (CL14, L57 to CL15, L5; CL15, L50-58; CL16, L48 to CL17, L38). **HE** teaches a co-simulation design system that provides for accurately simulating some of the bus transactions using a bus hardware model where the user may select the bus transactions to simulate (Fig 1, Item 124; Fig 16, Item 1603 and 1605; CL10, L23-32). **HE** does not expressly teach generating a test case for verification of the DUT by converting the condensed syntax into an enumeration of possible parameter

combinations for bus transactions of the DUT. **HU** teaches processing the configuration file to generate a test case for verification of the DUT (CL1, L64 to CL2, L5; CL2, L36-45), as that allows generating the tests in reduced time and the tests would exercise the device in a manner that was close to actual operation (CL2, L39-42), allowing the user to verify that the device meets all its functional requirements (CL2, L3-5). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the methods of **HE** comprising verification of the DUT by converting the condensed syntax into an enumeration of possible parameter combinations for bus transactions of the DUT with the method of **HU** that included processing the configuration file to generate a test case for verification of the DUT, as that would allow generating the tests in reduced time and the tests would exercise the device bus transactions in a manner that was close to actual operation allowing the user to verify that the bus transactions meet all functional requirements.

Per Claim 7: **HE** teaches that the syntax specifies a range of parameter values for the cache operations (CL14, L57 to CL15, L5; CL15, L50-58; CL16, L48 to CL17, L38). **SH** teaches a range of parameter values for the bus transactions (CL10, L44-67; CL11, L7-14), as the bus transaction parameters allow to appropriately configure the transaction to improve the efficiency of bus utilization (CL10, L48-50; CL11, L8-11). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of **HE** comprising syntax specifying a range of parameter values for the operations with the method of **SH** that included a range of parameter values for the bus transactions, as the bus transaction

parameters would allow to appropriately configure the transaction to improve the efficiency of bus utilization.

12. Claims 2, 6, 8, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hellestrand et al. (HE)** (U.S. Patent 6,263, 302) in view of **Apostol, Jr. et al. (AP)** (U.S. Patent 6,247,084) and **Sheafor et al. (SH)** (U.S. Patent 6,321,285), and further in view of **Huggins (HU)** (U.S. Patent 5,956,478) and **Shrote (SHR)** (U.S. Patent 5,774,358).

12.1 As per Claim 2, **HE, AP, SH** and **HU** teach the method of claim 1. **HE** teaches providing a design-under-test (DUT) configuration file comprising a specification of the model and parameters of the model and its operations corresponding to the DUT (CL14, L57 to CL15, L5; CL15, L50-58; CL16, L48 to CL17, L38); and a co-simulation design system that provides for accurately simulating some of the bus transactions using a bus hardware model where the user may select the bus transactions to simulate (Fig 1, Item 124; Fig 16, Item 1603 and 1605; CL10, L23-32). **HE** does not expressly teach that the processing step further comprises evaluating rules in the configuration file to include or exclude selected ones of the bus transactions from the test case. **HU** teaches that the processing step further comprises evaluating rules in the configuration file for automatically and randomly generating groups of tests (CL2, L35-39), as that allows generating the bus transaction test cases in reduced time and produces tests which exercise the device in a manner which is close to actual operation, to increase their effectiveness in testing (CL2, L41-45). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **HE** with the method of **HU**

that included the processing step further comprising evaluating rules in the configuration file for automatically and randomly generating groups of tests, as that would allow generating the bus transaction test cases in reduced time and would produce tests which exercised the device in a manner which was close to actual operation, to increase their effectiveness in testing.

SHR teaches that the processing step further comprises evaluating rules in the configuration file to include or exclude selected ones of the system elements from the test case (CL8, L19-33), as that allows generating the test instructions and data based on the particular rules provided by the user to meet the requirements of the test case (CL8, L26-28). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **HE** and **HU** with the method of **SHR** that included the processing step further comprising evaluating rules in the configuration file to include or exclude selected ones of the system elements from the test case, as that would allow generating the bus transaction test instructions and data based on the particular rules provided by the user to meet the requirements of the test case.

12.2 As per Claim 6, **HE, AP, SH** and **HU** teach the method of claim 5. **HE** teaches providing a design-under-test (DUT) configuration file comprising a specification of the model and parameters of the model and its operations corresponding to the DUT (CL14, L57 to CL15, L5; CL15, L50-58; CL16, L48 to CL17, L38). **HE** does not expressly teach including rules in the configuration file to include or exclude parameter combinations from the enumeration. **SHR** teaches including rules in the configuration file to include or exclude parameter combinations from the enumeration (CL8, L19-33), as that allows generating the test instructions and data

based on the particular rules provided by the user to meet the requirements of the test case (CL8, L26-28). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **HE** with the method of **SHR** that included rules in the configuration file to include or exclude parameter combinations from the enumeration, as that would allow generating the bus transaction test instructions and data based on the particular rules provided by the user to meet the requirements of the test case.

12.3 As per Claim 8, **HE, AP, SH** and **HU** teach the method of claim 5. **HE** does not expressly teach that the syntax specifies transaction types. **AP** teaches providing a specification of bus transaction types (Figs 8, 9 and 10; CL10, L55-60), as the bus supports different transaction types (CL10, L55). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of **HE** comprising a design-under-test (DUT) configuration file comprising a specification of the model and parameters of the model and its operations corresponding to the DUT and a co-simulation design system that provides for accurately simulating some of the bus transactions using a bus hardware model with the method of **AP** that included a specification of bus transaction types, as the bus would support different transaction types and the combination would allow the user to select the bus transactions to simulate using the specifications in the configuration file.

HE does not expressly teach a set of parameters for each transaction type. **SH** teaches a set of parameters for each transaction type (CL10, L44-67; CL11, L7-14), as the bus transaction parameters allow to appropriately configure the transaction to improve the efficiency of bus utilization (CL10, L48-50; CL11, L8-11). It would have been obvious to one of ordinary skill in

the art at the time of Applicants' invention to combine the method of **HE** comprising a design-under-test (DUT) configuration file comprising a specification of the model and parameters of the model and its operations corresponding to the DUT and a co-simulation design system that provides for accurately simulating some of the bus transactions using a bus hardware model with the method of **SH** that included a set of parameters for each transaction type, as the bus transaction parameters would allow to appropriately configure the transaction to improve the efficiency of bus utilization.

HE does not expressly teach directives for determining a mode of the converting. **SHR** teaches directives for determining a mode of the converting (Fig. 3A, Items 308 and 314; CL12, L37-43), as directives are input for particular tests to set the boundaries of testing and generate appropriate instruction/data stream for that test (CL12, L37-43). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of **HE** with the method of **SHR** that included directives for determining a mode of the converting, as directives would be input for particular tests to set the boundaries of testing and generate appropriate instruction/data stream for that test.

Per Claim 10: **HE** teaches that the directives cause values for the parameters to be evaluated as a list (CL14, L57-66).

12.4 As per Claim 11, **HE, AP, SH, HU** and **SHR** teach the method of claim 8. **HE** does not expressly teach that the directives cause the transaction types to be selected at random. **HU** teaches that the directives cause the transaction types to be selected at random (CL2, L35-42), as

that allows generating the tests that would exercise the bus transactions in a manner that was close to actual operation (CL2, L39-42), allowing the user to verify that the bus transactions meet all functional requirements (CL2, L3-5). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **HE** with the method of **HU** that included the directives causing the transaction types to be selected at random, as that would allow generating the tests that would exercise the bus transactions in a manner that was close to actual operation, allowing the user to verify that the bus transactions met all functional requirements.

13. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Hellestrand et al. (HE)** (U.S. Patent 6,263, 302) in view of **Apostol, Jr. et al. (AP)** (U.S. Patent 6,247,084) and **Sheafor et al. (SH)** (U.S. Patent 6,321,285), and further in view of **Huggins (HU)** (U.S. Patent 5,956,478), **Shrote (SHR)** (U.S. Patent 5,774,358) and **Mantooth et al. (MA)** (U.S. Patent 6,236,956).

13.1 As per Claim 9, **HE, AP, SH** and **HU** teach the method claim 1. **HE** does not expressly teach that the directives cause a value for the parameters to be stepwise incremented. **MA** teaches that the directives cause a value for the parameters to be stepwise incremented (CL10, L2-38; CL23, L40-67), as that allows predicting the effects of parameter variations on the system by simulation by sweeping the parameters within a range in a series of steps in which the specified parameter value is incremented by a predetermined increment until the specified range is completed (CL23, L44-52). It would have been obvious to one of ordinary skill in the art at

the time of Applicants' invention to modify the method of **HE** with the method of **MA** that included the directives causing a value for the parameters to be stepwise incremented, as that would allow predicting the effects of parameter variations on the system by simulation by sweeping the parameters within a range in a series of steps in which the specified parameter value is incremented by a predetermined increment until the specified range is completed.

14. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hellestrand et al. (HE)** (U.S. Patent 6,263, 302) in view of **Apostol, Jr. et al. (AP)** (U.S. Patent 6,247,084) and **Sheafor et al. (SH)** (U.S. Patent 6,321,285), and further in view of **Shrote (SHR)** (U.S. Patent 5,774,358) and **Meyer (ME)** (U.S. Patent 6,571,204).

14.1 As per Claim 12, **HE** teaches evaluating a syntax of a DUT configuration file including statements (CL14, L57 to CL15, L5; CL15, L50-58; CL16, L48 to CL17, L38); and a co-simulation design system that provides for accurately simulating some of the bus transactions using a bus hardware model where the user may select the bus transactions to simulate (Fig 1, Item 124; Fig 16, Item 1603 and 1605; CL10, L23-32). **HE** does not expressly teach defining transaction types and parameters corresponding to the DUT. **AP** teaches defining transaction types (Figs 8, 9 and 10; CL10, L55-60), as the bus supports different transaction types (CL10, L55). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the process of **HE** comprising evaluating a syntax of a DUT configuration file including statements with the process of **AP** that included defining transaction types, as the

bus would support different transaction types and the combination would allow the user to select the bus transactions to simulate using the specifications in the configuration file.

SH teaches defining parameters corresponding to the DUT (CL10, L44-67; CL11, L7-14), as the bus transaction parameters allow to appropriately configure the transaction to improve the efficiency of bus utilization (CL10, L48-50; CL11, L8-11). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the process of **HE** comprising evaluating a syntax of a DUT configuration file including statements with the process of **SH** that included defining parameters corresponding to the DUT, as the bus transaction parameters would allow to appropriately configure the transaction to improve the efficiency of bus utilization.

HE does not expressly teach a computer-usable medium storing computer-executable instructions, the instructions when executed implementing a process. **SHR** teaches a computer-usable medium storing computer-executable instructions, the instructions when executed implementing a process (Abstract, L1-4; Fig 6, Item 610; CL16, L57-67), as that would allow storing the computer readable instructions for directing the operation of the digital computer (CL16, L63-65). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the process of **HE** with the process of **SHR** that included a computer-usable medium storing computer-executable instructions, the instructions when executed implementing a process, as that would allow storing the computer readable instructions for directing the operation of the digital computer.

HE teaches evaluating a syntax of a DUT configuration file including statements (CL14, L57 to CL15, L5; CL15, L50-58; CL16, L48 to CL17, L38). **HE** does not expressly teach

generating bus functional language statements from the syntax. **ME** teaches generating bus functional language statements from the syntax (Fig. 2 and 3; CL5, L10-28; CL5, L40-50), as the bus functional language code executed by a controlling bus functional model (BFM) can be used to test the behavior of the device under test (CL5, L19-23). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the process of **HE** comprising evaluating a syntax of a DUT configuration file including statements with the process of **ME** that included generating bus functional language statements from the syntax, as the bus functional language code executed by a controlling bus functional model (BFM) could be used to test the behavior of the device under test.

14.2 As per Claim 13, **HE, AP, SH, SHR** and **ME** teach the computer-usable medium of claim 12. **HE** teaches a DUT configuration file including statements (CL14, L57 to CL15, L5; CL15, L50-58; CL16, L48 to CL17, L38); and a co-simulation design system that provides for accurately simulating some of the bus transactions using a bus hardware model where the user may select the bus transactions to simulate (Fig 1, Item 124; Fig 16, Item 1603 and 1605; CL10, L23-32). . **HE** does not expressly teach that the configuration file further includes rules for including or excluding selected bus functional language statements from being generated. **SHR** teaches that the configuration file further includes rules for including or excluding selected bus functions from being generated (CL8, L19-33), as that allows generating the test instructions and data based on the particular rules provided by the user to meet the requirements of the test case (CL8, L26-28). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the configuration file of **HE** with the configuration file of **SHR**

that included rules for including or excluding selected bus functions from being generated, as that would allow generating the bus transaction test instructions and data based on the particular rules provided by the user to meet the requirements of the test case.

HE does not expressly teach generating bus functional language statements from the rules. **ME** teaches generating bus functional language statements from the rules (Fig. 2 and 3; CL5, L10-28; CL5, L40-50), as the bus functional language code executed by a controlling bus functional model (BFM) can be used to test the behavior of the device under test (CL5, L19-23). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the process of **HE** comprising evaluating a syntax of a DUT configuration file including statements with the process of **ME** that included generating bus functional language statements from the rules, as the bus functional language code executed by a controlling bus functional model (BFM) could be used to test the behavior of the device under test.

14.3 As per Claim 14, **HE, AP, SH, SHR** and **ME** teach the computer-usable medium of claim 12. **HE** teaches that the evaluating and generating steps comprise testing a parameter combination generated from the configuration file (CL14, L57 to CL15, L5; CL15, L50-58; CL16, L48 to CL17, L38). **HE** does not expressly teach that the evaluating and generating steps comprise testing a parameter combination generated from the configuration file against the rules. **SHR** teaches that the evaluating and generating steps comprise testing a parameter combination generated from the configuration file against the rules (CL8, L19-33), as that allows generating the test instructions and data based on the particular rules provided by the user to meet the requirements of the test case (CL8, L26-28). It would have been obvious to one of ordinary skill

in the art at the time of Applicants' invention to modify the configuration file of **HE** with the configuration file of **SHR** that included the evaluating and generating steps comprising testing a parameter combination generated from the configuration file against the rules, as that would allow generating the bus transaction test instructions and data based on the particular rules provided by the user to meet the requirements of the test case.

HE teaches outputting the parameter combination in a bus functions (CL14, L57 to CL15, L5; CL15, L50-58; CL16, L48 to CL17, L38; CL10, L24-32). **HE** does not expressly teach outputting the parameter combination in a bus functional language statement when the parameter combination is not excluded by the rules. **ME** teaches outputting the parameter combination in a bus functional language statement when the parameter combination is not excluded by the rules (Fig. 2 and 3; CL5, L10-28; CL5, L40-50), as the bus functional language code executed by a controlling bus functional model (BFM) can be used to test the behavior of the device under test (CL5, L19-23). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the process of **HE** comprising outputting the parameter combination in a bus functions with the process of **ME** that included outputting the parameter combination in a bus functional language statement when the parameter combination is not excluded by the rules, as the bus functional language code executed by a controlling bus functional model (BFM) could be used to test the behavior of the device under test.

15. Claims 15, 16, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hellestrand et al. (HE)** (U.S. Patent 6,263, 302) in view of **Apostol, Jr. et al. (AP)** (U.S. Patent

6,247,084) and **Sheafor et al. (SH)** (U.S. Patent 6,321,285), and further in view of **Shrote (SHR)** (U.S. Patent 5,774,358).

15.1 As per Claim 15, **HE** teaches a system comprising a memory including computer executable instructions and a processor coupled to the memory for executing the instructions (Abstract, L1-6; Fig. 19; Cl5 L32-38; Cl14, L57-66); and

a system comprising a configuration file for a DUT (CL14, L57 to CL15, L5; CL15, L50-58; CL16, L48 to CL17, L38); wherein

the instructions process the configuration file to generate bus transactions for verification of the DUT (CL14, L57 to CL15, L5; CL15, L50-58; CL16, L48 to CL17, L38; CL10, L24-33).

HE does not expressly teach a configuration file for a DUT including bus transaction types and parameters corresponding to the DUT. **AP** teaches a configuration file for a DUT including bus transaction types (Figs 8, 9 and 10; CL10, L55-60), as the bus supports different transaction types (CL10, L55). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **HE** comprising the configuration file to generate bus transactions for verification of the DUT with the system of **AP** that included a configuration file for a DUT including bus transaction types, as the bus would support different transaction types and the combination would allow the user to select the bus transactions to simulate using the specifications in the configuration file.

SH teaches a configuration file for a DUT including parameters corresponding to the DUT (CL10, L44-67; CL11, L7-14), as the bus transaction parameters allow to appropriately configure the transaction to improve the efficiency of bus utilization (CL10, L48-50; CL11, L8-

11). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **HE** comprising the configuration file to generate bus transactions for verification of the DUT with the system of **SH** that included a configuration file for a DUT including parameters corresponding to the DUT, as the bus transaction parameters would allow to appropriately configure the transaction to improve the efficiency of bus utilization.

15.2 As per Claim 16, **HE, AP** and **SH** teach the system of claim 15. **HE** does not expressly teach that the configuration file includes rules for including or excluding selected bus transactions from being generated. **SHR** teaches that the configuration file includes rules to include or exclude selected ones of the system elements from the test case (CL8, L19-33), as that allows generating the test instructions and data based on the particular rules provided by the user to meet the requirements of the test case (CL8, L26-28). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **HE** with the system of **SHR** that included the configuration file including rules to include or exclude selected bus transactions from being generated, as that would allow generating the bus transaction test instructions and data based on the particular rules provided by the user to meet the requirements of the test case.

15.3 As per Claim 18, **HE** and **SHR** teach the method of claim 17. **HE** teaches a configuration file for a DUT (CL14, L57 to CL15, L5; CL15, L50-58; CL16, L48 to CL17, L38).

HE does not expressly teach that the configuration file includes statements defining transaction types to be generated and command statements which specify the parameters associated with each transaction type. **AP** teaches that the configuration file includes statements defining transaction types to be generated (Figs 8, 9 and 10; CL10, L55-60), as the bus supports different transaction types (CL10, L55). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **HE** comprising the configuration file with the method of **AP** that included the configuration file including statements defining transaction types to be generated, as the bus would support different transaction types and the combination would allow the user to select the bus transactions to simulate using the specifications in the configuration file.

SH teaches that the configuration file includes command statements which specify the parameters associated with each transaction type (CL10, L44-67; CL11, L7-14), as the bus transaction parameters allow to appropriately configure the transaction to improve the efficiency of bus utilization (CL10, L48-50; CL11, L8-11). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **HE** comprising the configuration file with the method of **SH** that included configuration file including command statements which specified the parameters associated with each transaction type, as the bus transaction parameters would allow to appropriately configure the transaction to improve the efficiency of bus utilization.

15.4 As per Claim 19, **HE, AP, SH** and **SHR** teach the method of claim 18. **HE** does not expressly teach that the command identifies a subset of the parameters which limits the number

of transactions in the test case. **SHR** teaches that the command identifies a subset of the parameters which limits the number of transactions in the test case (CL8, L19-33), as that allows generating the test instructions and data based on the particular rules provided by the user to meet the requirements of the test case (CL8, L26-28). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **HE** with the method of **SHR** that included the command identifying a subset of the parameters which limited the number of transactions in the test case, as that would allow generating the bus transaction test instructions and data based on the particular rules provided by the user to meet the requirements of the test case.

16. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Hellestrand et al. (HE)** (U.S. Patent 6,263, 302) in view of **Shrote (SHR)** (U.S. Patent 5,774,358).

16.1 As per Claim 17, **HE** teaches a method comprising preparing specifications of parameter combinations corresponding to buss transactions of a device under test (CL14, L57 to CL15, L5; CL15, L50-58; CL16, L48 to CL17, L38; CL10, L24-33); and

forming a configuration file of the parameter combinations in a condensed syntax including commands to select various parameter combinations (CL14, L57 to CL15, L5; CL15, L50-58; CL16, L48 to CL17, L38).

HE does not expressly teach generating a test case for a buss interface comprising including commands and rules to select various parameter combinations to be included in or excluded from the test case; and generating from the configuration file all bus transactions

defined by the rules comprising the test case. **SHR** teaches generating a test case for a buss interface comprising including commands and rules to select various parameter combinations to be included in or excluded from the test case; and generating from the configuration file all bus transactions defined by the rules comprising the test case (CL8, L19-33), as that allows generating the test instructions and data based on the particular rules provided by the user to meet the requirements of the test case (CL8, L26-28). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **HE** with the method of **SHR** that included generating a test case for a buss interface comprising including commands and rules to select various parameter combinations to be included in or excluded from the test case; and generating from the configuration file all bus transactions defined by the rules comprising the test case, as that would allow generating the bus transaction test instructions and data based on the particular rules provided by the user to meet the requirements of the test case.

HE does not expressly teach storing the bus transactions in an output file for use in a bus simulator. **SHR** teaches storing the bus transactions in an output file for use in a bus simulator (Fig 3B, Item 332; CL14, L25-27), as the output file can be used to verify bus transactions in a simulation (CL14, L30-32). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **HE** with the method of **SHR** that included storing the bus transactions in an output file for use in a bus simulator, as the output file could be used to verify bus transactions in a simulation.

Arguments

17.1 As per the applicant's argument that "In reviewing the primary reference to Hellestrand, ... While the ability to simulate the effects of a design on the bus hardware is disclosed in the reference, the reference fails to disclose how test cases can be made to completely test a design under test. In accordance with the foregoing, and the representative claims of the present application, a configuration file is formed of parameter combinations. From the configuration files, bus transactions can be defined by the rules comprising the test case. The bus transactions can then be stored in the output file for a bus simulator. In the Hellestrand reference, there doesn't appear to be any description of the kind of file or process for preparing the various test cases to test the bus transactions. While it is understood that the prior art discloses ways for creating bus transactions which can be used to verify a design under test, it is not clear from Hellestrand that there is any process or system which will create a configuration file as set forth in the rejected claims", the examiner has used **HE, HU** and **SHR** references which together perform these functions.

HE teaches providing a design-under-test (DUT) configuration file comprising a specification of model and parameters of the model and its operations corresponding to the DUT (CL14, L57 to CL15, L5; CL15, L50-58; CL16, L48 to CL17, L38); and a co-simulation design system that provides for accurately simulating some of the bus transactions using a bus hardware model where the user may select the bus transactions to simulate (Fig 1, Item 124; Fig 16, Item 1603 and 1605; CL10, L23-32). **HU** teaches that bus transactions can be defined by the rules comprising the test case and a process for preparing the various test cases to test the bus transactions from the rules (CL1, L64 to CL2, L5; CL2, L36-45). **SHR** teaches storing the bus transactions in an output file for use in a bus simulator (Fig 3B, Item 332; CL14, L25-27).

17.2 As per the applicant's argument that "In the Geer et al. reference, a system for generating various test cases to design an integrated circuit is shown. ... In reviewing the reference, it isn't clear where there is any process for creating bus transactions from a configuration file. While there are various tests implemented to check a simulated circuit design, nothing appears in the reference to suggest that bus transactions are created from a configuration file of parameters, and used to verify the device under test", the examiner has used the **HE, AP** and **SH** references which together perform this function.

HE teaches providing a design-under-test (DUT) configuration file comprising a specification of model and parameters of the model and its operations corresponding to the DUT (CL14, L57 to CL15, L5; CL15, L50-58; CL16, L48 to CL17, L38); and a co-simulation design system that provides for accurately simulating some of the bus transactions using a bus hardware model where the user may select the bus transactions to simulate (Fig 1, Item 124; Fig 16, Item 1603 and 1605; CL10, L23-32). **AP** teaches providing a specification of bus transaction types (Figs 8, 9 and 10; CL10, L55-60). **SH** teaches providing a specification of bus transaction parameters (CL10, L44-67; CL11, L7-14).

17.3 As per the applicant's argument that "The addition of a Huggins reference fails to disclose any configuration file which is capable of generating bus transactions. ... Given the fact that the reference does not deal with generating bus transactions, so that a device under test may be fully tested, it is not seen how it can be combined with the foregoing references to render this subject matter obvious. Column 2, lines 35-39, while alluding to the prior art process of

generating an automated test case, fails to disclose a generation of a set of transactions from a configuration file where various parameters are stored with rules to define the particular bus transactions of the test", the examiner has used the **HE** and **HU** references which together perform these functions.

HE teaches providing a design-under-test (DUT) configuration file comprising a specification of model and parameters of the model and its operations corresponding to the DUT (CL14, L57 to CL15, L5; CL15, L50-58; CL16, L48 to CL17, L38); and a co-simulation design system that provides for accurately simulating some of the bus transactions using a bus hardware model where the user may select the bus transactions to simulate (Fig 1, Item 124; Fig 16, Item 1603 and 1605; CL10, L23-32). **HU** teaches that bus transactions can be defined by the rules comprising the test case and a process for preparing the various test cases to test the bus transactions from the rules (CL1, L64 to CL2, L5; CL2, L36-45).

17.4 As per the applicant's argument that "The El-Ghoroury et al. reference describes the architecture and design of an application specific processor. The design originates from various programmable application elements which can be selected to create a specific application. In viewing the reference, there isn't any description of any bus transactions which can be used to verify a test case", the examiner has used the **HE, AP** and **SH** references which together perform this function as shown in Paragraph 17.2 above.

17.5 As per the applicant's argument that "In reviewing Hellestrand et al. (U.S. Patent 6,263,302), Geer et al. and El-Ghouroury et al. references, it is not seen where there is any

method disclosed which would generate bus transactions from a configuration file of stored parameter values. Accordingly, the combination of references could not yield or disclose these features of Applicants' rejected claims", the examiner has used the **HE, AP** and **SH** references which together perform this function as shown in Paragraph 17.2 above.

17.6 As per the applicant's argument that "The Hellestrand et al., Geer et al., El-Ghouroury et al. and Apostol, Jr. et al. (U.S. Patent 6,247,084) and Sheafor et al. (U.S. 6,321,285) references also fail to disclose any type of bus transaction which can be created from a configuration file of parameter combinations. Accordingly, the combination fails to suggest these elements of Applicants' claims as well", the examiner the examiner has used the **HE, AP** and **SH** references which together perform this function as shown in Paragraph 17.2 above.

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
June 10, 2004

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER